

## CLAIMS

What is claimed is:

- 1 1. A system, comprising:  
2 a bus;  
3 first logic to generate a multiphase encoded waveform; and  
4 second logic coupled to the first logic to drive the multiphase encoded  
5 waveform onto the bus.
- 1 2. The system of claim 1 wherein the first logic includes a multiphase phase lock  
2 loop to generate multiple phases for the multiphase encoded waveform.
- 1 3. The system of claim 1 wherein second logic includes third logic to generate  
2 differential signal levels representing the multiphase encoded waveform.
- 1 4. The system of claim 2 wherein the first logic includes an input register, coupled  
2 to the multiphase phase lock loop, to receive at least one data word or at least one  
3 command/control word.
- 1 5. The system of claim 4 wherein the input register comprises a first-in-first-out  
2 (FIFO) register.
- 1 6. The system of claim 4 wherein the input register includes a command/control  
2 signal input, wherein a command/control signal on the command/control signal input  
3 is to indicate whether the multiphase encoded waveform is a data structure or a  
4 command/control structure.

1 7. The system of claim 3 wherein the bus includes at least one differential  
2 transmission line to receive signal levels for the multiphase encoded waveform.

1 8. The system of claim 7 wherein second logic further comprises impedance  
2 matching circuitry to match impedance of the second logic to the differential  
3 transmission line.

1 9. The system of claim 1, further comprising third logic coupled to the bus to  
2 receive the multiphase encoded waveform.

1 10. The system of claim 9 wherein the third logic includes an amplifier to receive  
2 differential signal levels representing the multiphase encoded waveform from the bus  
3 and extract the multiphase encoded waveform from the received differential signal  
4 levels.

1 11. The system of claim 10 wherein the third logic includes a differential delayed  
2 lock loop coupled to stretch a multiphase encoded waveform timing to a  
3 predetermined length.

1 12. The system of claim 11 wherein the third logic includes a register coupled to  
2 check data integrity of the multiphase encoded waveform.

1 13. An apparatus, comprising:  
2 a device driver having first logic to generate a multiphase encoded  
3 waveform and second logic coupled to the first logic to drive the multiphase encoded  
4 waveform onto a bus.

1 14. The apparatus of claim 13 wherein the first logic includes a multiphase phase  
2 lock loop to generate multiple phases for the multiphase encoded waveform.

1 15. The apparatus of claim 13 wherein second logic includes third logic to generate  
2 differential signal levels representing the multiphase encoded waveform.

1 16. The apparatus of claim 14 wherein the first logic includes an input register,  
2 coupled to the multiphase phase lock loop, to receive at least one data word or at least  
3 one command/control word.

1 17. The apparatus of claim 14 wherein the input register comprises a first-in-first-  
2 out (FIFO) register.

1 18. The apparatus of claim 15 wherein the input register includes a  
2 command/control signal input, wherein a command/control signal on the  
3 command/control signal input is to indicate whether the multiphase encoded  
4 waveform is a data structure or a command/control structure.

1 19. The apparatus of claim 13 wherein second logic further comprises impedance  
2 matching circuitry to match impedance of the second logic to a bus differential  
3 transmission line.

1 20. An apparatus, comprising:

2 a device driver to receive a multiphase encoded waveform, having:

3 an amplifier to receive differential signal levels representing the  
4 multiphase encoded waveform from the bus and extract the multiphase encoded  
5 waveform from the received differential signal levels; and

6 a differential delay-lock loop coupled to stretch the received  
7 multiphase encoded waveform timing to a predetermined length.

1 21. The apparatus of claim 20, further comprising a register coupled to check data  
2 integrity of the received multiphase encoded waveform.

1 22. The apparatus of claim 21 wherein the register includes logic to extract data  
2 bits from the received multiphase encoded waveform and to perform a probability  
3 analysis to determine a likelihood of errors.

1 23. The network of claim 20 wherein the differential delay-lock loop includes logic  
2 to align rising edges of the received multiphase encoded waveform to rising edges of a  
3 transmitted multiphase encoded waveform.